Impact on Power System Dynamics of PI Control Limiters of VSC-based Devices

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***Abstract*—This paper presents and compares a variety of PI controllers with different implementations of windup and anti-windup limiters. The paper shows that a precise modeling of these controllers is of crucial importance for an accurate prediction of the dynamic response of power systems that operate close to their operational limits. The focus is on PI controllers included in voltage sourced converters. In particular, the case study considers two relevant applications of such devices, namely the Static Synchronous Compensator and a Multi-terminal Direct Current grid.**

***Index Terms*—PI controller, anti-windup limiter, Voltage Source Converter (VSC), Static Synchronous Compensator (STATCOM), Multi-terminal Direct Current (MTDC).**

I. Introduction

A. Motivation

PI controllers are ubiquitous in power systems due to their simple structure, easy tuning and overall good dynamic performance. Among their numerous applications, PI controllers are particularly common in power electronics-based devices, such as Flexible AC Transmission System (FACTS) devices and, more recently, distributed energy resources connected to the grid through Voltage Sourced Converters (VSCs).

While the normal operation of PI controllers is univocal and straightforward to implement, there is no commonly accepted standard for the implementation of hard limits on PI controllers. This modeling uncertainty is particularly critical for VSC-based applications where it is crucial to keep the currents of the converter within their operational limits. Also, due to the open access market and integration of stochastic renewable energy, power systems are currently often operated closer to their limits.

Figure 1 shows a real-world example of such a situation, where the High Voltage Direct Current (HVDC) links of Great Britain are operated at their limits for a significant period of time during daily operation [1]. Another example is the voltage collapse reported in [2] that was caused by the field current limiters of synchronous generators. It is thus widely recognized the crucial importance of taking into account control limits, in particular when dealing with power

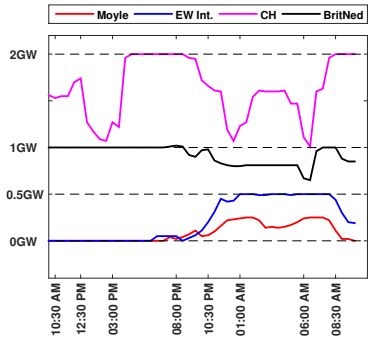

Figure 1: Power flow through the HVDC links of Great Britain: Moyle (0.5 GW), EastWest Interconnector (0.5 GW), HVDC Cross-Channel (CH, 2 GW) and BritNed (1 GW) in July 03-04, 2017 [1].

electronics devices, for an accurate dynamic assessment of power systems [3]. This paper addresses the modeling issue of PI controllers from a simulation point of view and studies the impact of different implementations of PI limiters on the dynamic response of power systems.

B. Literature Review

PI controllers with windup or anti-windup strategies are used in various power system applications, such as FACTS devices [4], VSCs [5], IEEE standard excitation system models ST4C, ST6C, ST8C, AC7C and AC11C [6], standard model for type-III wind turbine generators developed by the Western Electricity Coordinating Council (WECC) [7], among others. If the limiting action (anti-windup) in the PI controller model is considered, it becomes a hybrid (non-smooth) dynamical system [8]. Therefore, to capture the actual physical dynamics, the anti-windup strategy of PI controllers should be properly modeled. This modeling issue is widely studied and numerous strategies have been proposed, e.g., in [9], [10]. While IEEE standard proposes only one anti-windup limiter model [6], the power system community has adopted other alternative implementations depending on the application: VSC-based HVDC control [11], [12]; FACTS devices [13]; energy storage-based control [14]; and automatic generation control [15].

C. Paper Contribution

The effects of PI control limiters on the dynamic performance of power systems has been studied for some specific application. For example, in [16], the authors discussed the *field oriented control* of permanent magnet synchronous machines. However, a systematic study of the impact of different

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modeling approaches of PI controller limits on the transient response of power systems has not been conducted thus far. This paper fills this gap and thoroughly discusses the effect of different PI limiter models on the dynamic response of benchmark power system networks. The contributions of this paper are twofold:

- To present windup and anti-windup PI control modeling strategies for power system applications.
- To study the effect on the power system dynamic performance of the limiters of PI controllers of VSC devices considering FACTS and HVDC link applications.

D. Paper Organization

The remainder of this paper is organized as follows. Section II provides a brief overview of modeling approaches of PI controllers with and without hard limits. Section III presents the model of the VSC along with its regulator schemes and limiting strategies. The dynamic performance of each limiter model is compared in the case study presented in Section IV, based on two applications, namely, the STATCOM device and a benchmark MTDC grid. In Section V a brief discussion of simulation results is given. Finally, in Section VI, conclusions and future work directions are drawn.

II. PI CONTROL

The Proportional, Integral and Differential (PID) control is one of the most common control strategies for a huge variety of practical applications [17]. However, systems characterized by the presence of noise and by the occurrence of large disturbances such as power systems, the derivative component can deteriorate the performance of the controller, and thus, of the overall system. Therefore, the derivative component of PID controllers is often not included in power system applications. In the remainder of this paper, thus, we focus exclusively on PI controllers.

A. Modeling of PI Controllers

The transfer function $G(s)$ of a PI controller without any constraint shown in Fig. 2(a) is given by:

$$G(s) = K_p + \frac{K_i}{s} \ , \tag{1}$$

where K_p and K_i are the proportional and integral gains of the controller, respectively. The PI controllers are configured in two different ways: (a) Analog, based on Operational Amplifiers (OP-Amps) [18]; and (b) Digital, based on Field Programmable Gate Array (FPGA) [19]. However, there are significant differences in the implementations of the limiters in both configurations, in particular anti-windup ones, of PI controllers. Most common solutions are presented below.

1) Windup integrator: This model limits the output of the PI control and thus the integral action is continuous or smooth. This model is shown in Fig. 2(b) and given by:

$$\begin{aligned} y &= K_p u + x \\ \dot{x} &= K_i u \ , \end{aligned} \tag{2}$$

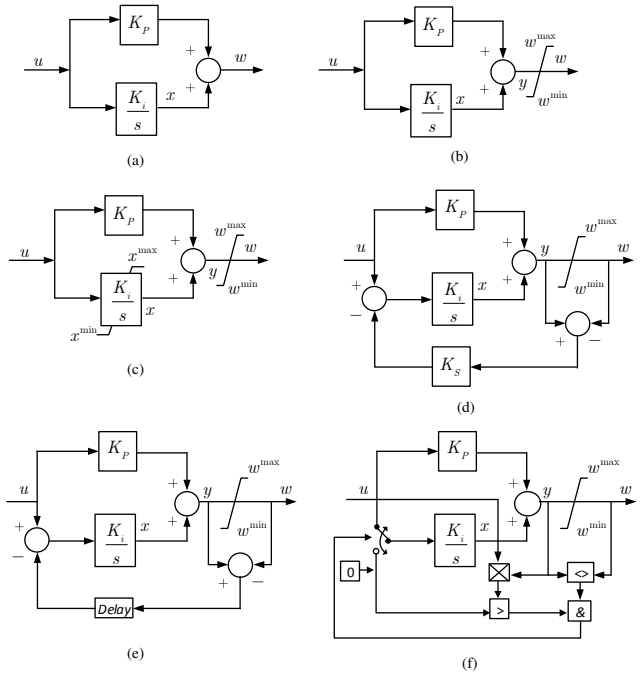

Figure 2: PI controller: (a) without limits (b) windup limiter (c) limited integrator (conditional integrator) (d) back calculation or tracking anti-windup with high feedback gain (e) tracking anti-windup with delay (f) integrator clamping.

where u is the input to the PI controller; y is the output without limits and x is the state variable of the integrator. The output of the PI controller w is:

$$w = \begin{cases} w_{\text{max}} & \text{if } y \geq w_{\text{max}} \ , \\ y & \text{if } w_{\text{min}} < y < w_{\text{max}} \ , \\ w_{\text{min}} & \text{if } y \leq w_{\text{min}} \ . \end{cases} \tag{3}$$

2) Conditional integrator: This model disables the integrator within the controller when the output of the controller is beyond the limits. IEEE standard uses the conditional integrator, shown in block diagram in Fig. 2(c) to define the anti-windup PI control (without the limits on the state x) [6]. Mathematically, the model given by IEEE standard is as follows:

$$\begin{aligned} &\text{If } y \geq w_{\text{max}} : w = w_{\text{max}} \text{ and } \dot{x} = 0 \ , \\ &\text{If } y \leq w_{\text{min}} : w = w_{\text{min}} \text{ and } \dot{x} = 0 \ , \\ &\text{Otherwise} : w = y = K_p u + x \text{ and } \dot{x} = K_i u \ . \end{aligned} \tag{4}$$

Considering that the integrator is also limited [20], [21] (see Fig. 2(c)), the integrator model becomes:

$$\begin{aligned} &\text{If } x \geq x_{\text{max}}, \text{ and } \dot{x} \geq 0 \ : x = x_{\text{max}} \text{ and } \dot{x} = 0 \ , \\ &\text{If } x \leq x_{\text{min}}, \text{ and } \dot{x} \leq 0 \ : x = x_{\text{min}} \text{ and } \dot{x} = 0 \ , \\ &\text{Otherwise} : \dot{x} = K_i u \ . \end{aligned} \tag{5}$$

3) Back calculation: Back calculation consists of measuring the error between w and y and using it as a feedback signal to compensate the input to the integrator [11], [22], [23]. This method is also called *tracking anti-windup with high gain* or

TABLE I: List of PI controller models.

Model	Description
PI 1	No limits considered (1)
PI 2	Only output is limited (2) - (3)
PI 3	Hard limits on state and output (4) - (5)
PI 4	IEEE standard (4)
PI 5	Back calculation with gain (6)
PI 6	Back calculation with delay (7)
PI 7	Combined conditional and back calculation (8)

anti-reset windup, depicted in Fig. 2(d). Mathematically, the integrator equation is given by:

$$\dot{x} = K_i[u - K_s(y - w)] \ , \tag{6}$$

where K_s is the feedback gain. The block in Fig. 2(e) considers a feedback with delay and this model is used in power system simulation tool EMTP-RV [24]. The integral action is given by:

$$\dot{x}(t) = K_i[u(t) - v(t - \tau)] \ , \tag{7}$$

where $v(t) = y(t) - w(t)$ is the feedback signal and τ is the time delay.

4) Combined conditional and back-calculation: This approach also known as *integrator clamping* has been proposed in [9], [25]. The summing point that performs the feedback to the integral term is replaced by a switch. Depending on the conditions (8), the switch position is changed, shown in Fig. 2(f). This approach can be stated as:

$$\begin{gathered} \text{If } y \neq w, \text{ and } uy > 0 \ : \dot{x} = K_i[u + (w - y)] \ , \\ \text{Otherwise} : \dot{x} = K_i u \ . \end{gathered} \tag{8}$$

B. Comparison of PI Controller Outputs

Seven PI controller configurations are considered in this work, as shown in Table I. The dynamic responses of these controllers are compared by giving a sinusoidal input and using the Modelica language in OpenModelica [26]. The results of this comparison are shown in Fig. 3. The differences among the outputs are fairly small, when limits are binding. Nevertheless, Fig. 3 shows only the output of the PI controllers. How these differences affect the behavior of an interconnected system cannot be known *a priori*. In other words, the impact of nonlinearity on the dynamic behavior of a complex system cannot be anticipated, as the case study of this paper thoroughly illustrates.

III. Voltage Sourced Converter

VSCs are power electronic devices utilized to convert electrical energy from AC to DC or *vice versa*. To study the dynamic interactions of the VSC-based devices, different modeling strategies are adopted [5]. In electromechanical models, where the fast switching of converters are ignored, VSC models are approximated using Average Value Models (AVM) [27], [28]. The AVM model of the VSC device and its regulators is well-assessed for the transient stability studies considered in the paper, and is presented in the remainder of this section.

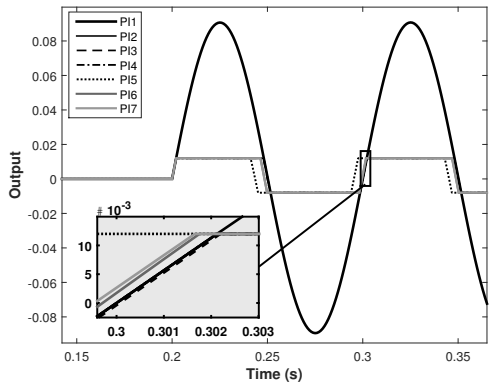

Figure 3: Transient response of the 7 PI controller configurations considered in this paper (see Table I).

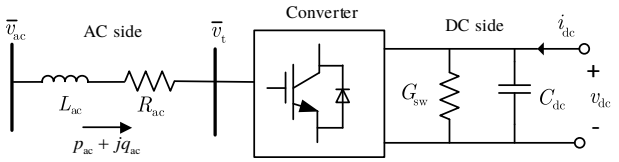

Figure 4: VSC scheme interfacing a DC grid with an AC grid.

A. Dynamic Model of the VSC for Transient Stability Analysis

The usual configuration of a VSC is depicted in Fig. 4 [29]. This configuration includes a transformer in the AC side, a bi-directional converter and a condenser. The conversion of DC voltage to AC voltage is done by the power electronic switches, which are controlled by appropriate control logic.

The dynamics of the AC side of the VSC considering a rotating dq-frame are given by [28]:

$$\begin{aligned} R_{\text{ac}} i_{\text{ac,d}} + L_{\text{ac}} \frac{di_{\text{ac,d}}}{dt} &= \omega_{\text{ac}} L_{\text{ac}} i_{\text{ac,q}} + v_{\text{ac,d}} - v_{\text{t,d}} \\ R_{\text{ac}} i_{\text{ac,q}} + L_{\text{ac}} \frac{di_{\text{ac,q}}}{dt} &= -\omega_{\text{ac}} L_{\text{ac}} i_{\text{ac,d}} + v_{\text{ac,q}} - v_{\text{t,q}} \ , \end{aligned} \tag{9}$$

where $R_{\text{ac}} + jL_{\text{ac}}$ is the aggregated impedance of the converter and transformer impedances; ω_{ac}, v_{ac}, i_{ac} and v_{t} are the frequency, AC grid voltage, AC side current and AC terminal voltage, respectively. The power balance between the AC and DC sides of the converter is given by:

$$p_{\text{ac}} + v_{\text{dc}} i_{\text{dc}} - p_{\text{loss}} - \frac{1}{2} C_{\text{dc}} \frac{d(v_{\text{dc}}^2)}{dt} = 0 \ , \tag{10}$$

where $p_{\text{ac}} = (\frac{3}{2})(v_{\text{ac,d}} i_{\text{ac,d}} + v_{\text{ac,q}} i_{\text{ac,q}})$; $\frac{1}{2} C_{\text{dc}} \frac{d(v_{\text{dc}}^2)}{dt}$ is the energy variation in the capacitor; $p_{\text{loss}} = (\frac{3}{2}) R_{\text{ac}} i_{\text{ac}}^2 + G_{\text{sw}} v_{\text{dc}}^2$ are the circuit and switching losses of the converter respectively, with $i_{\text{ac}}^2 = i_{\text{ac,d}}^2 + i_{\text{ac,q}}^2$ and G_{sw} is obtained from a given constant conductance G_0 and the quadratic ratio of the actual current to the nominal one, as follows [29]:

$$G_{\text{sw}} = G_0 \left(\frac{i_{\text{dc}}}{i_{\text{dc}}^{\text{nom}}} \right)^2 \ . \tag{11}$$

The AC quantities are expressed in the dq-reference frame, achieved through a Phase-Locked Loop (PLL) [30]. The PLL forces the angle of the dq-frame to track the angle θ_{ac}.

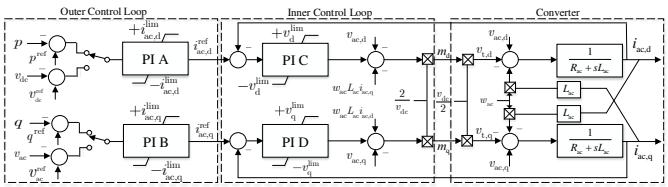

Figure 5: VSC converter, outer control and inner current control in dq-frame.

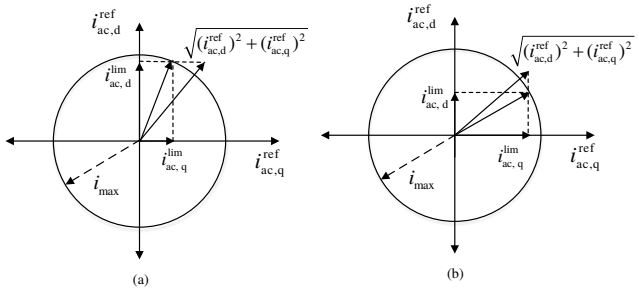

Figure 6: Current limiting strategies: priority given to: (a) d-axis current; and (b) q-axis current.

B. Control Structure

Figure 5 shows the control structure of the VSC considered in this paper. The VSC includes outer and inner controllers (see Fig. 5) [11], [12], [31]. Each converter station can control active power (p) or DC voltage (v_{dc}), as well as the reactive power (q) or AC voltage (v_{ac}) by means of two decoupled control loops. The control structure is implemented in such a way that it can be used in all possible configurations. All controllers are PI controllers.

C. Current Limiting Strategies

Active and reactive power transfer capabilities are always limited for VSC-based devices [32]. One way to impose such limitation is by using over-current limiters in the outer control. Different strategies are utilized to calculate the current limits in the outer control system [33]. When giving priority to active power over reactive power as shown in Fig. 6(a), $i^{\text{ref}}_{\text{ac, d}}$ is limited to the maximum current capacity $\pm i_{\text{max}}$ and $i^{\text{ref}}_{\text{ac, q}}$ is limited in such a way that the total current does not exceed the maximum current rating of the valves, as follows:

$$\begin{aligned} i^{\text{lim}}_{\text{ac, d}} &= i_{\text{max}} \\ i^{\text{lim}}_{\text{ac, q}} &= \sqrt{i^2_{\text{max}} - i^2_{\text{ac, d}}}\ . \end{aligned} \tag{12}$$

Similarly, higher priority to reactive power over active power can be applied, as shown in Fig. 6(b).

IV. Case Study

Two applications of VSC-based devices, namely, FACTS (STATCOM) and MTDC links, are considered in Subsections IV-A and IV-B, respectively, to investigate the seven PI control configurations defined in Section II. The focus is on the impact of PI control limiters and, hence, no other grid limits are considered. The Python-based software Dome [34] has been used to implement all PI models and to simulate the case studies considered in this paper.

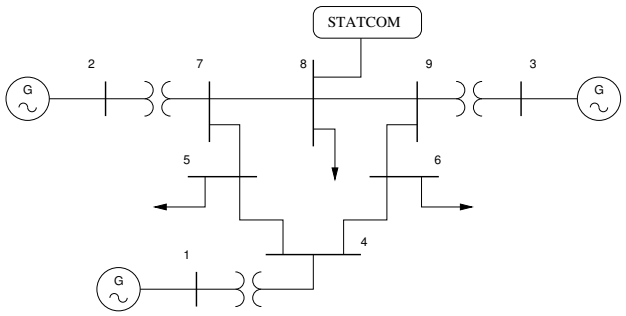

Figure 7: WSCC 9-bus test system with a VSC-based STATCOM connected at bus 8.

TABLE II: STATCOM parameters.

Name	Values
VSC Rating	± 95 MVA
Transformer	$x_{\text{t}} = 0.401$ pu, $r_{\text{t}} = 0.003$ pu
Current Limits	$i_{\text{max}} = 1.01$ pu, $i_{\text{min}} = -0.80$ pu
Outer Control	$K^{\text{A}}_p = 50$, $K^{\text{B}}_p = 60$, $K^{\text{A}}_i = 25$, $K^{\text{B}}_i = 35$
Inner Control	$K^{\text{C}}_p = 0.2$, $K^{\text{D}}_p = 0.2$, $K^{\text{C}}_i = 20$, $K^{\text{D}}_i = 20$
Other	$K_s = 50$, $\tau = 0.01$ s

A. STATCOM

The STATCOM is a shunt-connected FACTS device, utilized to regulate the voltage of the bus where it is connected. Therefore, except for some small losses, only reactive power is exchanged between the AC system and the STATCOM device [20]. The WSCC 9-bus test system (see Fig. 7) with a VSC-based STATCOM, connected at bus 8 is used for time domain simulation. The test network consists of three synchronous machines, three two-winding transformers, three loads and six transmission lines. All generators are equipped with Automatic Voltage Regulators (AVRs) and Turbine Governors (TGs). The dynamic data of this test network is provided in [35]. The STATCOM rating is taken from [36] and the parameters used are given in Table II. The current limit is set by giving priority to reactive power.

The STATCOM connected at bus 8 regulates the DC and AC side voltages. Therefore, there are four PI controllers in operation in the test network, two in the outer level and two in the inner level of the STATCOM (see Fig. 5). The reference voltages set for v_{ac} and v_{dc} are 1.015 and 1 pu, respectively.

1) Contingency: A three phase fault at bus 6 was simulated at $t = 1$ s and cleared after 60 ms through disconnecting the line that connects buses 6 and 9. Simulation is carried out considering both the upper and lower current limits (see Table II) of the PIs (PI 2 - PI 7) controlling AC and DC voltages. The trajectories of the voltage at bus 8 ($v_{\text{Bus 8}}$) and q-axis current reference ($i^{\text{ref}}_{\text{ac,q}}$) are shown in Figs. 8 and 9, respectively, for the different PI controller configurations.

The response of PI 1 (no limits) is used as reference for the comparison. PI 2 - PI 4 provide fairly similar transient responses. On the other hand, PI 5 - PI 6 consider a feedback when the output hits the limit, so the non-zero feedback signal

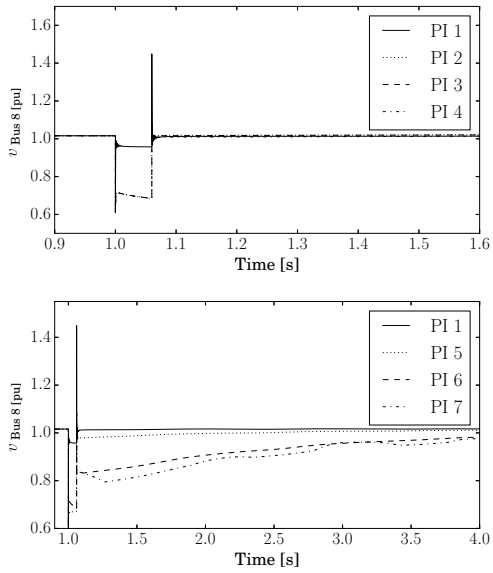

Figure 8: Response of the bus voltage $v_{\text{Bus 8}}$ of the WSCC 9-bus system: using PI 1 - PI 4 (top); using PI 1 and PI 5 - PI 7 (bottom).

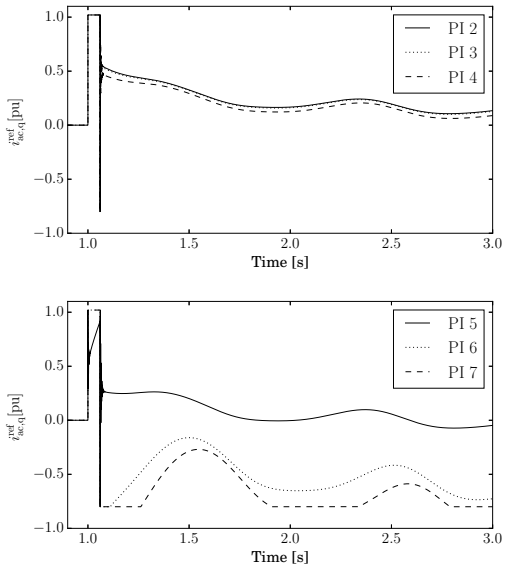

Figure 9: Response of the q-axis current reference of STATCOM ($i_{\text{ac, q}}^{\text{ref}}$) in the WSCC 9-bus system: using PI 2 - PI 4 (top) and using PI 5 - PI 7 (bottom).

drives the integrator in order to restore the output to within limit, so these models provide similar transient responses. Also, due the feedback gain in PI 5, the current reference is rapidly driven back to within limits (see Fig. 9). For all the PI types the current reference converges to steady state, however for PI 6 and PI 7 the convergence is slower compared to others. PI 7 displays a relatively different transient response in the controlled variable due to the second condition (8). It is evident from Figs. 8 and 9 that there is a considerable difference in the transient behavior when considering different anti-windup strategies (PI 3 - PI 7).

2) Effect of feedback gain (PI 5) : The response of the WSCC 9-bus test system facing a three phase fault using

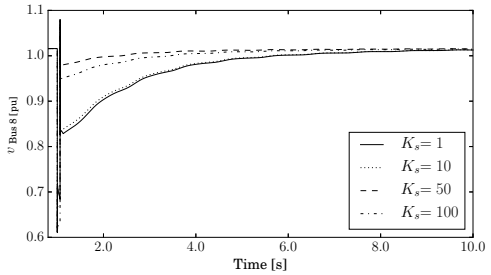

Figure 10: Response of the bus voltage $v_{\text{Bus 8}}$ of the WSCC 9-bus system using PI 5 with different feedback gain.

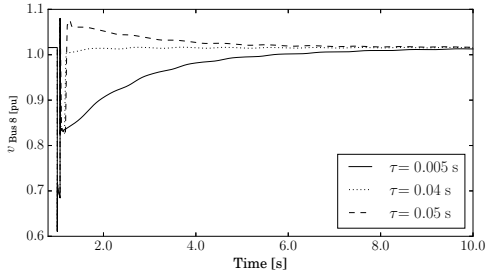

Figure 11: Response of the bus voltage $v_{\text{bus 8}}$ of the WSCC 9-bus system using PI 6 with different feedback delay.

different K_s of the PI 5 is now studied. The trajectories of the bus voltage ($v_{\text{Bus 8}}$) are shown in Fig. 10. It can be seen that there are differences in the trajectories due to the different values of the feedback gain parameter. To ensure a relatively fast response of the integrator, it is recommended to use a higher value of this feedback gain. Nevertheless a higher feedback gain does not ensure a better transient response (see Fig. 10). So it is important to tune this parameter appropriately.

3) Effect of time delay (PI 6): The PI 6 configuration given by equation (7) has a feedback delay (τ). The sensitivity of the dynamic response of PI 6 with respect to the delay is now studied by applying the three phase fault using different τ's. The bus voltage ($v_{\text{Bus 8}}$) trajectories are shown in Fig. 11. Note that different values of τ imply considerably different transient responses.

B. MTDC Grid

DC electric networks connected with more than two terminal converter stations are known as MTDC grids [28]. In this section, the MTDC grid with four DC stations involving three asynchronous AC areas shown in Fig. 12 is used for the case study. This test system was originally given in [28]. In this paper, a modified version proposed in [37] is considered. The VSC models and their controllers are replaced with those described in Section III. In nominal conditions, two converter stations (DC Node 1 and 4) are considered to be acting as rectifiers (AC to DC) and the others (DC Node 2 and 3) as inverters (DC to AC). All AC generators are synchronous machines equipped with AVRs, TGs and modeled using the sixth order generator models provided in [20]. The DC line resistance and capacitance used are $R_{\text{dc}ij} = 1.5\,\Omega$, $C_{\text{dc}ij} = 0.4$

TABLE III: HVDC link configurations at nominal condition.

Name	VSC 1	VSC 2	VSC 3	VSC 4
DC Node	1	2	3	4
AC Bus	16	13	12	14
Type	Rectifier	Inverter	Inverter	Rectifier
Control	v_{dc} and v_{ac}	p and v_{ac}	p and v_{ac}	p and v_{ac}
Reference	$v_{\text{dc}}^{\text{ref}} = 1.0$ $v_{\text{ac}}^{\text{ref}} = 0.99$	$p^{\text{ref}} = -8.96$ $v_{\text{ac}}^{\text{ref}} = 0.96$	$p^{\text{ref}} = -2.96$ $v_{\text{ac}}^{\text{ref}} = 0.98$	$p^{\text{ref}} = 9.0$ $v_{\text{ac}}^{\text{ref}} = 0.99$

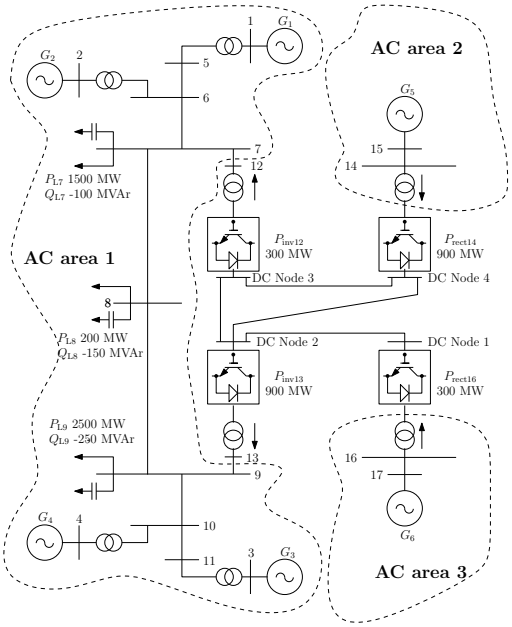

Figure 12: MTDC grid connected to multi-machine AC system.

mF respectively for every line connections between DC node i and j, while HVDC link settings are given in Table III.

1) Contingency: A three-phase fault occurs at bus 8 at 0.2 s and is cleared after 60 ms. Since the system topology is not changed after clearing the fault, the system is expected to restore its previous stable equilibrium after the transient. The outer control limits are imposed based on converter rating and priority is given to active power. During the fault, AC voltage controller (VSC 3) and active power controller (VSC 2 and VSC 3) hit the limit. The trajectories of bus voltage 12 and active power injection of VSC 2 are shown in Figs. 13-14. Comparing simulation results, the transient responses are different.

V. Discussion of Implementation issues and simulation results

The following remarks are relevant.

- The PI 1 model is certainly adequate for small signal stability analysis. However, for transient stability analysis it is important to take into account control limits.
- PI 2 can be used in situations where no anti-windup function is necessary. However, for most power system applications this model is not recommended because of the effect of the integrator windup.
- PI 3 and PI 4 consider anti-windup limits by conditional integration, being the latter recommended by IEEE

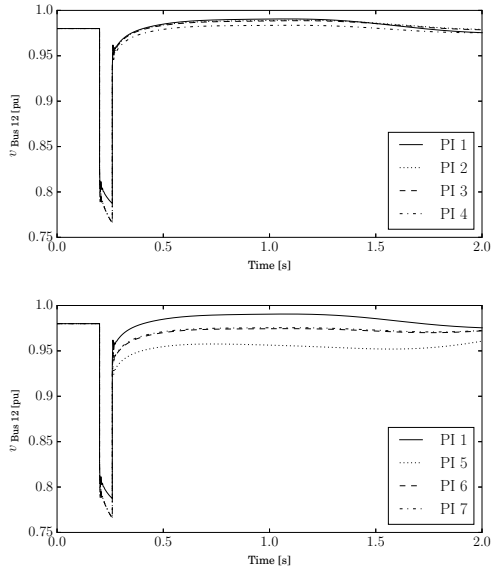

Figure 13: Bus voltage $v_{\text{Bus 12}}$ response of the MTDC grid: using PI 1 - PI 4 (top); using PI 1 and PI 5 - PI 7 (bottom).

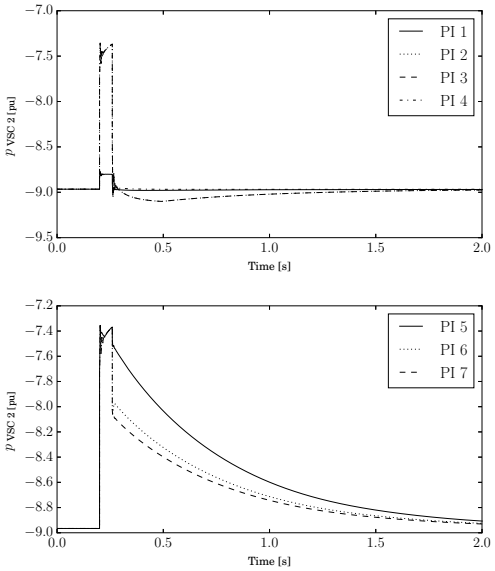

Figure 14: Active Power response of VSC 2 of the MTDC grid: using PI 1 - PI 4 (top) and using PI 5 - PI 7 (bottom).

standard. However, due to the dynamic interaction of continuous state and discrete events induced by limits, the Jacobians of the DAEs need to be re-factorized during the time domain simulation. This refactorization can cause numerical issues [38].

- PI 5 and PI 6 implement an anti-windup limiter through a feedback signal, with two advantages: (a) they try to restore the current reference (see Fig. 9) within their limits so that power electronic switches will not be stressed for a long time; and (b) the integral action given by (6) is continuous w.r.t. the conditional integral model given by (4) so there is no need to re-factorize the Jacobian matrix. There are also two disadvantages of using these models: (a) they require one extra parameter

(back calculation gain, K_s and feedback delay, τ) to tune; and (b) when a limit is binding, the dynamic response of these models can worsen the overall behavior of the controlled variable.

- PI 7 has similar features and provides a similar response as PI 5 and PI 6. It is, however, more complicated to implement as it includes several discrete variables which can lead to numerical issues.

VI. Conclusion

The paper shows that different implementations of PI control limiters result in significantly different transient responses of interconnected power systems. Among the considered implementations of the anti-windup types, we identify two main groups based on their characteristic features: (i) conditional integration (PI 3 and PI 4); and feedback-type integrators (PI 5 - PI 7). It is important to note that the IEEE standard includes only one anti-windup PI model which belongs to the first group.

Future work will extend this study by implementing the all-island Irish transmission system with HVDC interconnections and show the effect of anti-windup limiters for large disturbances and power transfer ramps between Ireland and the UK system. Other relevant aspects to be considered in future work are the dynamic interaction of controller and grid limits, and the optimal design of PI parameters. Also, future study will consider Stochastic Differential Equations (SDEs) and discuss recommendations on the modeling of PI anti-windup limiters for power system transient stability analysis.

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